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Radiation Effects in 3D Integrated SOI SRAM Circuits

DTRA Approved

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Abstract – Radiation effects are presented for the first time for vertically integrated 3 x 64-kb SOI SRAM circuits fabricated using Lincoln 3DIC technology. Three fully-fabricated 2D circuit wafers are stacked using standard CMOS fabrication techniques including thin-film planarization, layer alignment and oxide bonding. Micron-scale dense 3D vias are fabricated to interconnect circuits between tiers. Ionizing dose and single event effects are discussed for proton irradiation with energies between 4.8 and 500 MeV. Results are compared with 14-MeV neutron irradiation. Single event upset cross-section, tier-to-tier and angular effects are discussed. The interaction of 500-MeV protons with tungsten interconnects is investigated using Monte-Carlo simulations. Results show no tier to tier effects and comparable radiation effects on 2D and 3D SRAM. 3DIC technology is a potential candidate for fabricating circuits for space applications.

Index Terms—single event effects, SOI, fully depleted, 3D integration, neutron, protons, upset cross-section

I. INTRODUCTION

3D integrated circuits are an emerging technology to continue improving system performance beyond the end of Moore's Law [1]. This approach can significantly increase integration density, reduce interconnection length and enable integration of heterogeneous materials, technologies and functionality components in a monolithically integrated process. Lincoln Laboratory has developed a wafer-based 3D technology that enables stacking of multiple IC wafers (or tiers) [2]. This approach is well suited for high-density stacking of heterogeneous technologies because the substrates from the stacked tiers are removed, and oxide-through vias are used for short electrical interconnects. Several designs have been demonstrated including a large-area 8x8 mm²

high-3D-via-count 1024 x 1024 visible imager [3], a 64 x 64 laser-radar focal plane based on single-photon-sensitive avalanche photodiodes [4], a 10Gb/s/pin low power interconnect for 3DICs [5], and an imaging array with InP diode and Si CMOS readout tiers [6]. We reported earlier that total ionizing dose (TID) effects in n-channel FETs (nFETs) in the bottom tier were similar to those on standard single tier wafers [7],[8]. Less positive charge build-up was observed for wide nFETs on the upper tiers, which was associated with the absence of silicon material below the BOX.

This paper reports for the first time on the radiation effects in SOI SRAM circuits that are vertically integrated on three tiers. TID effects, low-to-high energy proton and 14.5 MeV neutron irradiation data are discussed. We found that both neutrons and proton irradiation effects in the 3D SOI SRAM circuits are similar to those on a single tier 2D SOI SRAM. The other tiers can be effectively modeled as a modified backend of line (BEOL) stack. Angular effects are consistent with a cosine angular dependence. Monte Carlo simulations were performed to analyze the effects tungsten contacts and vias had on tier-to-tier energy deposition. We also demonstrate that the current 3DIC process is tolerant to TID.

II. 3D FABRICATION PROCESS

The three-tier Integrated Circuits (ICs) characterized in this work were fabricated in the third DARPA-sponsored 3D multiproject run (3DM3). The process begins with fabricating three 150-mm individual tiers of fully depleted SOI (FDSOI) circuit tiers, with a 150-nm FET gate length, 40-nm-thick SOI active layer and a 400-nm buried oxide (BOX), a dual threshold CMOS, Co-silicided polygates with a silicide block layer, and three metal interconnect layers. The circuits were designed using standard logic design rules. Specific alignment structures were added to the lithographic masks to enable accurate tier-to-tier alignment (<+/- 0.75 μ m). The 3D integration begins with oxide-oxide bonding of tier-1 and tier 2 wafers. The tier 2 substrate is then removed by grinding and wet chemical

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etching, stopping on the tier-2 SOI buried oxide layer. Electrical interconnection is formed by through-oxide vias to tier 2, 3D vias from tier-1 to tier-2, and a tier-2 back metal layer. The process is then repeated with tier 3. An illustrated cross-section of a 2D integrated circuit and a 3DIC wafer is shown in Figure 1. 3D-IC with eleven interconnect-metal layers and dense unrestricted 1.25- μm -diameter 3D via interconnecting stacked circuit layers. The SRAM active circuitry is confined within a 20- μm -thick layer above the SOI substrate. Figure 2 shows an illustration of the 2D and 3D integrated circuit cross-section. Figure 2 shows a scanning electron micrographs of a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D vias interconnecting tiers 1, 2 and 3.

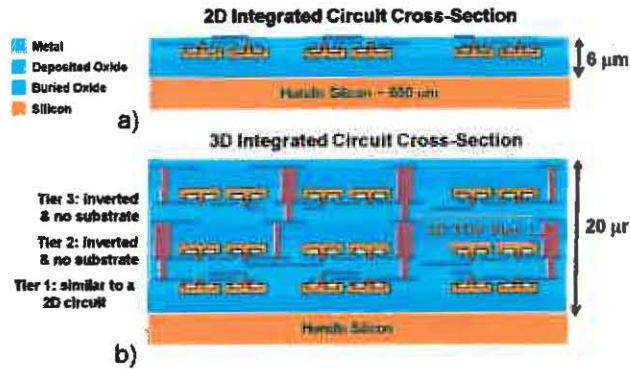


Figure 1: Illustrated cross-section of a) a 2D integrated circuit and b) a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D Through Oxide Vias (TOV) interconnecting tiers 1, 2 and 3.

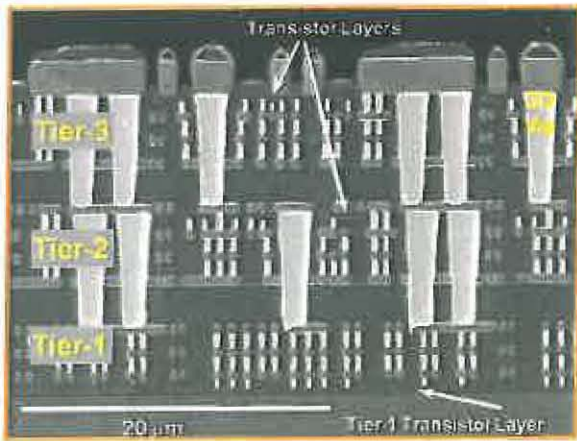


Figure 2: Scanning Electron Micrographs of a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D vias interconnecting tiers 1, 2 and 3.

Upon completion of single tier fabrication and again after 3D integration, an extensive series of tests is performed to characterize passive test structure, transistor and circuit performance to monitor the effect

of wafer integration. Figure 3 shows $I_{\text{drain}}(V_{\text{gate}})$ curves at $V_{\text{drain}} = 1.5 \text{ V}$ for $W=8 \mu\text{m}$, $L=0.15 \mu\text{m}$ transistors on tiers 1, 2, & 3 after 2D fabrication and after 3D integration. The $I_{\text{drain}}(V_{\text{gate}})$ characteristics for tiers 1, 2, & 3 are essentially unchanged by the 3D process, although FETs on each tier have somewhat different electrical characteristics.

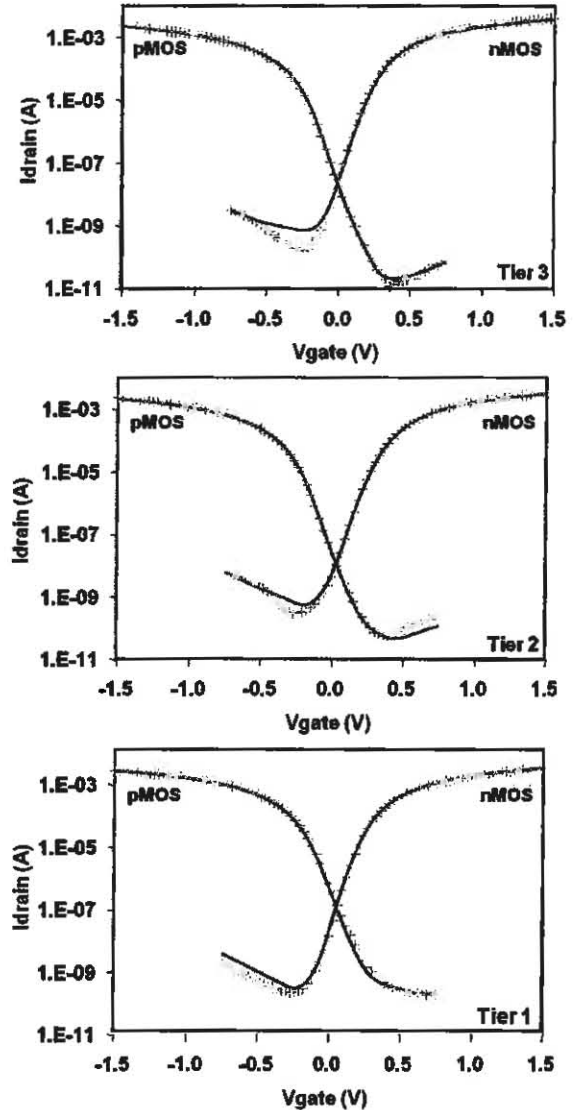


Figure 3: $I_{\text{drain}}(V_{\text{gate}})$ curves at $V_{\text{drain}} = 1.5 \text{ V}$ for $W=8 \mu\text{m}$, $L=0.15 \mu\text{m}$ FETs on tiers 1, 2, & 3 before (symbols) and after (solid line) 3D integration.

III. CIRCUIT DESCRIPTION AND RADIATION TESTING EXPERIMENTS

A. Circuit description

The baseline 64-kb SRAM core is organized as a 512-row by 128-column array, includes fully-static CMOS decoders, and an address re-encoder for

testability and variable timing. Data are accessed via 4-bit buses, using 14-bit addressing. The SRAM cell has 6 transistors with n-channel FET pass-gates, and conventional transistor layout with no body ties. It is not optimized for speed or power, and it is primarily used for circuit validation and fabrication debugging.

The 3D SOI SRAM consists of three instantiations of the 64-kb SRAM core, multiplexed to operate as a single memory. The total memory size is 192-kb, with tier selection controlled by two additional pads. Figure 4 shows an illustrated cross-section of a 3D SOI SRAM. The SRAMs on tier 3, tier 2 and tier 1 are located 2,600 nm, 9,900 nm and 20,350 nm, respectively, below the passivation surface. The SRAMs on tier 2 and 3 are inverted compared to that on tier 1. The tier-to-tier circuit alignment is a function of the wafer-to-wafer alignment during tier integration, and it is nominally $\pm 0.75 \mu\text{m}$. Figure 4 also shows that the 3D tungsten-filled vias are located a minimum of $\sim 230\text{-}\mu\text{m}$ from the SRAM bit cells; that is much longer than the range of low-energy secondaries generated by the particle (proton or neutron) -silicon nuclear interactions. Therefore the interaction of radiation with the 3D vias will not be discussed in the manuscript. However standard tungsten-contacts and vias are used throughout the SRAM circuit and are located less than $0.5 \mu\text{m}$ away from the cell FET active region. Their impact on the radiation effects will be discussed in section V.

Figure 5 shows a side-by-side illustrated cross-section of a 2D and 3D SRAM. The tier 1 of the 3D SOI SRAM is similar to the baseline single-tier 2D SRAM. Two variants of the 2D SRAM were tested. Each variant used a different substrate for CMOS circuit fabrication: a standard commercial SOI wafer with a standard buried oxide (STD) and a Lincoln-fabricated SOI wafer with a buried oxide hardened to ionizing radiation (RAD). The SOI wafer used for the tier 1 circuit fabrication of the 3D SOI SRAM was also a Lincoln-fabricated SOI wafer.

The 2D and 3D SOI SRAM circuits were packaged in a 40-pin dual in-line package. The package lead was removed during all the irradiation tests. Circuits were irradiated under constant biasing of 1.25 V, with a back substrate voltage at 0-V and no lid on the package. The upset cross-section in cm^2/bit was calculated by dividing the total number of upsets by the particle fluence and the total number of bits.

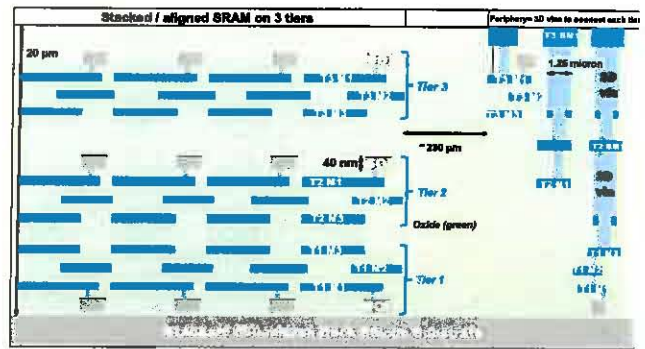


Figure 4: Illustrated cross-section of MITLL 3DSOI SRAM circuit. The 3D vias are small enough to be useful in large numbers inside circuits, but for this application they were only needed in the periphery. "BM" stands for Back Metal layer ("Back") because it is on the back of the SOI.

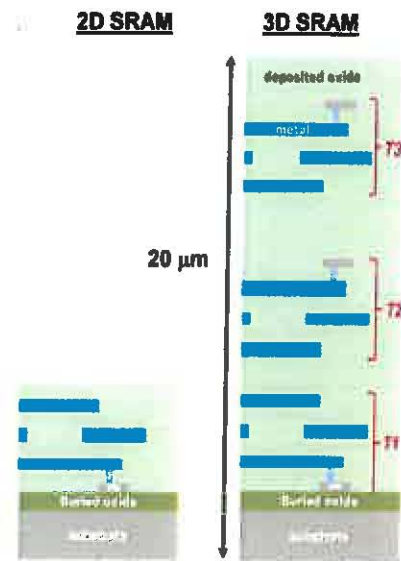


Figure 5: Side-by-side illustrated cross-section drawn to scale of MITLL 2D and 3D SOI SRAM Circuits.

B. Proton Upset Measurements

Circuits were irradiated at the TRIUMF Proton Irradiation Facility in Vancouver, Canada [9]. This facility provides mono-energetic proton beams from 63 to 500 MeV with energies down to 4.8 MeV obtained by degrading the 63-MeV low energy beam. Table 1 lists the beam Full-Width-Half-Max (FWHM) for the proton fluences of 63 MeV and below. Proton fluxes up to $10^{11} \text{ cm}^{-2} \text{ s}^{-1}$ can be achieved with uniform beams up to 7.5 cm in diameter.

Table 1: Proton beam Full-Width-Half-Max (FWHM) for the proton fluences of 63 MeV and below.

Proton Test Energy (MeV)	Energy FWHM (MeV)
63	1.2
57.6	1.4
50	
48.8	1.7
35.5	2.5
27.1	2.9
20.7	3.3
13.7	4.6
9	6
4.8	5.7

SRAMs were tested at room temperature in the static mode before and after radiation increments using an FPGA board remotely controlled from a laptop. The FPGA test board was ~ 5 feet away from the irradiated test board. It was shielded with polyethylene blocks, and kept sufficiently far away from the proton beam to prevent radiation damage. A checkerboard pattern of “0” and “1” was written and read right before irradiation. Then, the memory was read right after irradiation as soon as the proton beam was turned off. Because of the memory size and the small sensitive volume of the FDSOI cell transistors (defined by the area under the gate, *i.e.*, ~ 750-nm x 150-nm x 40-nm for the cell), proton fluences ~ $1 \times 10^{11} \text{ cm}^{-2}$ were required to measure a statistically meaningful number upsets without accumulating too much total dose. Standard unhardened FDSOI technology is sensitive to ionizing radiation because of charge trapped in the BOX below the active SOI layer [10]. Because of the front-to-back capacitive coupling, significant device parametric shifts can be observed unless the BOX has been engineered to mitigate these effects as with the Lincoln-fabricated SOI wafers [11]. The I_{DD} supply current was measured before and after irradiation each irradiation. SRAM circuits were irradiated at proton incident angles between 0 and 80°. Then the test board was turned 180° for irradiation from the backside.

C. 14-MeV Neutron Upset Measurements.

Another set of SRAM circuits were exposed to 14 MeV neutrons. These circuits were from the same fabrication lots as the one used for the proton testing. These measurements were performed using the neutron generator at the U.S. Naval Academy.

The generator is a broad beam source that uses the deuterium-tritium reaction to produce 14-MeV neutrons. The SRAMs were tested in the static mode before and

during irradiation with the same FPGA board setup used for the proton measurements. A checkerboard pattern of “1” and “0” was written to the memory before turning the neutron beam on. With the beam still on, the memory was read at specific fluence increments up to total fluences between 5 and $10 \times 10^{12} \text{ n/cm}^2$. The neutron flux was $2.08 \times 10^8 \text{ n/cm}^2/\text{s}$ for all irradiation at angles between 0 and 80°. It was $1.11 \times 10^8 \text{ n/cm}^2/\text{s}$ for irradiation at 180°.

IV. RESULTS

A. Proton-induced Upsets

Ionizing dose effects: the total ionizing dose increases with an increase in proton fluence; therefore it is important to identify any circuit parametric shifts caused by the cumulated proton fluence. The total cumulated dose is worst for proton energies of 500 MeV. This may be due to a higher charge yield for the very high energy proton irradiation [12].

Figure 6 shows the I_{DD} supply current measured after radiation increments for the 2D-STD and 2D-RAD, and the 3D SOI SRAM for a proton energy of 500 MeV. The 2D-STD SRAM has an I_{DD} current that increases starting at 30 krad (Si), while it remains unchanged for 2D RAD and the 3DSOI SRAM. This is because, as the proton fluence increases, positive charge builds-up in the BOX. This charge decreases the nFET threshold voltage thereby increasing its off-state leakage current. Consequently the I_{DD} current increases with the proton fluence. The Lincoln-fabricated wafer used for fabricating the 2D-RAD SRAM is effective in suppressing ionizing dose effects, and the I_{DD} remains constant with an increase in proton fluence. The I_{DD} current of the 3DSOI SRAM remains also unchanged with total dose indicating that the FETs on all three tiers are tolerant to ionizing effects. This is explained because a) tier 1 circuits were fabricated with a Lincoln-fabricated wafer with an engineered hardened BOX, and b), as shown in previous work, FETs on tiers 2 and 3, which had the silicon substrate removed, are much less sensitive to total dose effects than those on a standard single tier wafer [8]. These results indicate that the TID hardness of the 3D SRAM is better than 100 krad (Si), which is the calculated cumulated dose at a proton fluence of $2.5 \times 10^{11} \text{ p/cm}^2$.

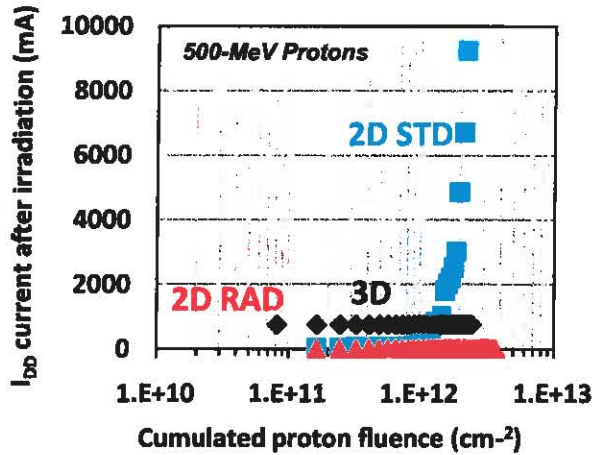


Figure 6: I_{DD} supply current for 2D-STD, 2D-RAD 64-kb and 3D 192-kb SOI SRAM measured after radiation increments as a function of the cumulated 500-MeV proton fluence.

Proton upset cross-section: 500-MeV proton-induced upsets were measured for 2D and 3D SOI SRAM circuits at multiple proton fluences. Measurements were repeated. Table 2 shows the median upset cross-section calculated from the experimental data for 2D-STD, 2D-RAD and tier 1 of 3D-SRAM (3D-Tier1). As we will discuss in the next section, the three SRAM circuits have comparable upsets cross-sections.

Table 2: Experimental median cross-section with 500-MeV protons for 2D standard (2D-STD), 2D-RAD and tier 1 of 3D-SRAM (3D-Tier1).

CM ² /BIT	2D-STD	2D-RAD	3D-TIER1
MEDIAN σ_{SEU}	1.84×10^{-14}	1.6×10^{-14}	1.99×10^{-14}
STD.DEV.	2.11×10^{-15}	1.87×10^{-15}	1.28×10^{-15}

Figure 7 shows the median upset cross-section for the SRAM on tier 1, 2 and 3 of the 3DIC as a function of the proton energy. The median upset cross-section is lower on tier 2 compared to that on tiers 1 and 3 regardless of the proton incoming angle. We will show in the next section that the difference in upset cross-section measured for each tier is not significant enough to conclude that we have different effects on each tier or even tier to tier effects.

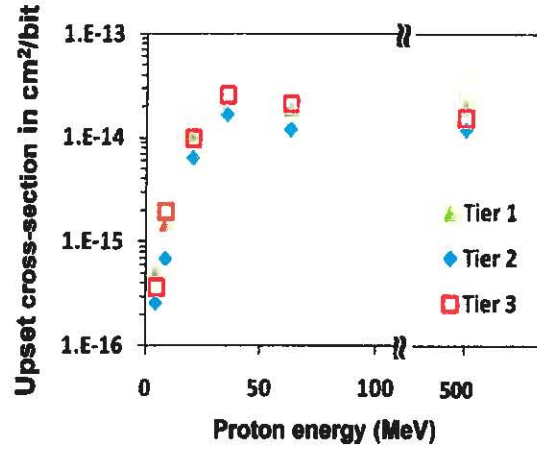


Figure 7: Median upset cross-section for tier 1, 2 and 3 of 3D SOI SRAM as a function of the proton energy.

Angular effects: Figure 8 shows the median upset cross-section for tier 1, 2 and 3 of a 3DSOI SRAM calculated from experimental measurements as a function of the incident angle, θ , for 500-MeV protons. θ is in the plane of the gate length as shown on the illustrated cross-section of an FDSOI FET inserted on the plot. The error bars are the standard deviation of repeated measurements and multiple circuits. The upset cross-section increases with the particle incident angle. Front and back irradiations yield similar cross-sections on each tier, with no significant differences between tiers. Note that at 180° , the protons are going through the board and the package.

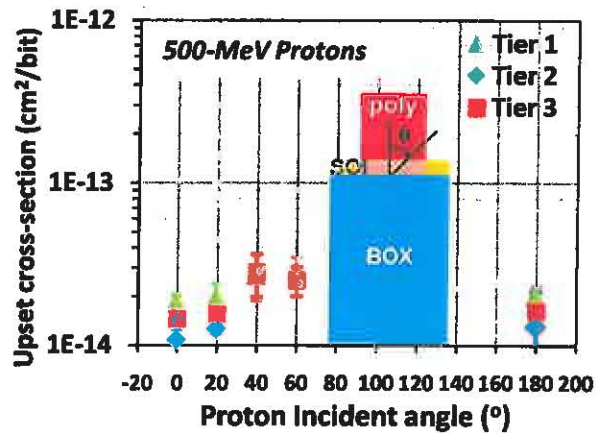


Figure 8: Experimental median upset cross-section for tiers 1, 2 and 3 of a 3DSOI SRAM as a function of the 500-MeV proton incident angle, θ , in the plane of the gate length as shown with the illustrated cross-section of a FDSOI FET. The error bars are the standard deviation of repeated measurements.

Figure 9 shows the upset cross-section for tiers 1, 2 and 3 of a 3D SOI SRAM as a function of the 63-MeV proton incident angle. The upset cross-section increases with θ . The results are similar to those shown for 500-MeV protons in Figure 8.

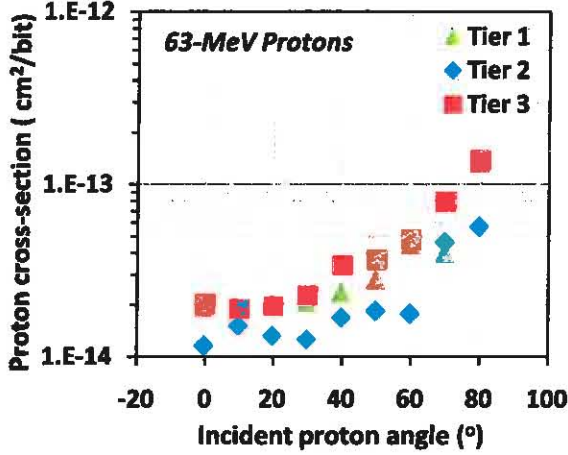


Figure 9: Experimental upset cross-section for tiers 1, 2 and 3 of 3DSOI SRAM as a function of the 63-MeV proton incident angle, θ , in the plane of the gate length.

B. Neutrons-induced Upsets

Figure 10 shows the typical number of upsets recorded for a 2D-STD and 2D-RAD SRAM as a function of the neutron fluence.

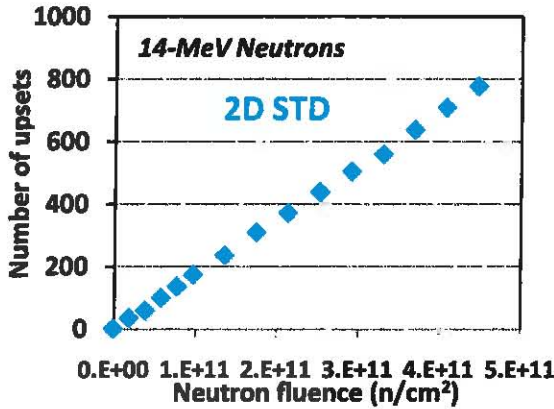


Figure 10: Typical upsets versus neutron fluence for a 2D-STD SRAM.

14-MeV neutron cross-section and angular effects: 2D and 3D SRAMs were irradiated under various θ angles in the plane of the gate length. Figure 11 shows the neutron upset cross-section for each tier and for various neutron incident angles. The upset cross-

section for 2D and 3D SRAM is similar. For each incident angle, the upset cross-section is similar on tier 1, 2 and 3, and it is similar to that for 2D SRAM. Experimental results show that the tier 2 SRAM have a lower cross-section than the other two tiers for all particle incident angle, but as we will discuss in the next section, the difference is not significant enough to conclude that radiation effects are different on tier 2 compared to the other tiers.

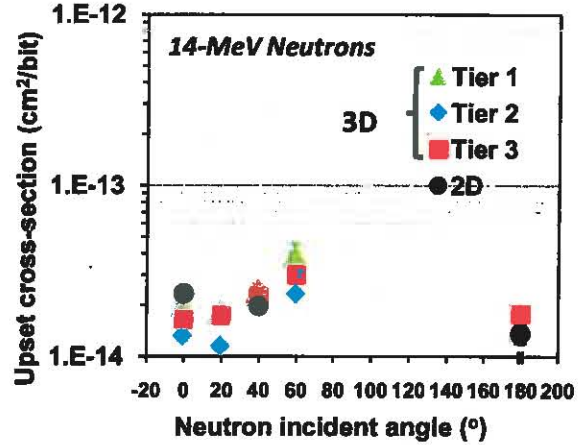


Figure 11: Median upset cross-section for 2D-SRAM and for tiers 1, 2 and 3 of 3DSOI SRAM as a function of the 14-MeV neutron incident angle, θ , in the plane of the gate length.

V. RESULTS ANALYSIS AND DISCUSSION

First we will compare test results for the 2D and 3D-tier1 SRAM to assess if the difference in the measured upset cross-sections is significant enough to conclude that the 3D integration process has an impact on the radiation effects. Then we will analyze and discuss the protons and neutrons data, and the angular effects. We will compare results for tiers 1, 2 and 3 of the 3D SOI SRAM, and present simulation results for the energy deposited by 500-MeV protons in the sensitive regions of the 3D stack.

A. Comparing 2D and 3D-Tier 1 SRAM

For FDSOI, the FET sensitive volume in the SRAM cell is the device area right under the gate. It is very small, and we define it here as $L \times W \times T_{\text{SOI}}$ where L is the gate length, W is the gate width, and T_{SOI} is the SOI thickness. Figure 12 shows a 3D illustrated representation of a FDSOI FET with a sensitive volume of $L \times W \times T_{\text{SOI}}$ where $W = 0.75 \mu\text{m}$, $L = 0.15 \mu\text{m}$, $\text{SOI} = 0.04 \mu\text{m}$. Just considering variations in L and W allowed during the photolithography of the gate pattern, $\Delta L_{\text{max/min}} = \pm 0.015 \mu\text{m}$, and W , $\Delta W_{\text{max/min}} = \pm 0.05 \mu\text{m}$,

across a wafer within a lot or from lot-to-lot, we calculated the minimum and maximum upset cross-section defined as:

$$\sigma_{\min} = [(\Delta L - L) \times (\Delta W - W)] / (\text{total number of bits}) \quad (1)$$

and

$$\sigma_{\max} = [(\Delta L + L) \times (\Delta W + W)] / (\text{total number of bits}) \quad (2)$$

where $L = 0.15 \mu\text{m}$ and $W = 0.75 \mu\text{m}$.

Table 3 shows that σ_{\min} is $1.44 \times 10^{-14} \text{ cm}^2/\text{bit}$ and σ_{\max} is $2.01 \times 10^{-14} \text{ cm}^2/\text{bit}$. The median upset cross-sections measured for 2D-STD, 2D-RAD and 3D-Tier 1 reported in Table 1 for 500-MeV protons are well within the range defined by σ_{\min} and σ_{\max} , therefore differences in the values are just indicative of variations in the fabrication process. As previously shown in [13], process variations tend to dominate variations in experimental cross-section data in advanced SOI technologies. This result is not specific to Lincoln-fabrication process. It is common to all advanced technologies currently in the research and development stage.

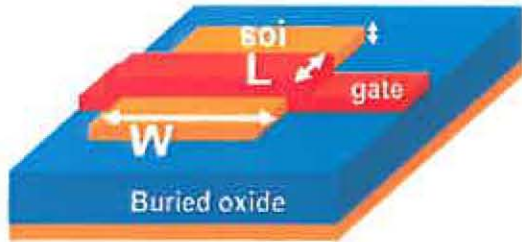


Figure 12: Illustrated 3D view of a FDSOI FET with a sensitive volume of $W \times L \times \text{SOI}$ where $W = 0.75 \mu\text{m}$, $L = 0.15 \mu\text{m}$, $\text{SOI} = 0.04 \mu\text{m}$

Table 3: Minimum and maximum upset cross-sections calculated considering variation in the sensitive area defined as $W \times L$ where W is the device gate width, and L gate length. Here $L = 0.15 \mu\text{m}$ and $W = 0.75 \mu\text{m}$; $\Delta W = 0.05 \mu\text{m}$ and $\Delta L = 0.015 \mu\text{m}$. The nominal upset cross-section is $1.72 \times 10^{-14} \text{ cm}^2/\text{bit}$.

Minimum and maximum sensitive device area	Calculated upset cross-section for a minimum (cm^2/bit)
$(L-dL) \times (W-dW)$	1.44×10^{-14}
$(L+dL) \times (W+dW)$	2.01×10^{-14}

B. Comparing Neutrons and Protons Data

Monoenergetic neutrons and protons are used to characterize single event effects in electronics circuits, and are described in the JEDEC JESD 89 standard [14]. With both particles, upsets are generated by the

secondary ion distribution due to the proton-nuclei and neutron-nuclei interactions. Proton- and neutron-induced upset cross-sections are often found to be similar, but the accuracy of the results depends strongly on the availability of high particle fluxes. Consequently protons are used for energies greater than 50 MeV. However, protons can have two important disadvantages: protons can be attenuated if the package is too thick, and they can contribute to total ionizing dose effects.

Our experimental measurements did not show a significant difference between the protons and neutrons induced upset cross-sections for all the tiers of the 3D SOI SRAM – at least within the accuracy of our measurements. This is in agreement with the results in Figure 6 showing that the 3D SOI SRAM is not sensitive to the ionizing dose cumulated during proton irradiation. Also, the SRAM package is not thick enough to attenuate the protons.

Figure 7 shows that the proton LET threshold is lower than $10 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ for all the tiers of the 3D SOI SRAM as expected from previously published results for 2D SOI SRAM [15]. This is also agreement with the reported sensitivity to 14-MeV neutrons producing ions with LET of $\sim 7 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

C. Analyzing Angular Effects

Table 2 shows that the particle path length in the sensitive volume increases as a function of the incident angle. Its increase is proportional to inverse-cosine of the particle incident angle, *i.e.* $1/\cos\theta$. To analyze the proton and neutron angular effects, we calculated the upset cross-section at an angle θ , $\sigma(\theta)$, as being equal to be equal to $\sigma(0)/\cos\theta$, where $\sigma(0)$ is the upset cross-section measured at a normal incidence angle. Figure 13 shows the experimental and the calculated upset cross-section for tier 1 of 3D SOI SRAM as a function of the 500-MeV proton incident angle. Experimental data follow the trend predicted by the inverse-cosine calculation. Note that few data are available reporting angular effects for FDSOI SRAM.

Table 2: Particle path length in the sensitive volume as a function of the particle incident angle.

ANGLE (°)	PARTICLE PATH LENGTH IN THE SENSITIVE VOLUME (NM)
0	40
20	42.6
40	52.2
60	80
80	230

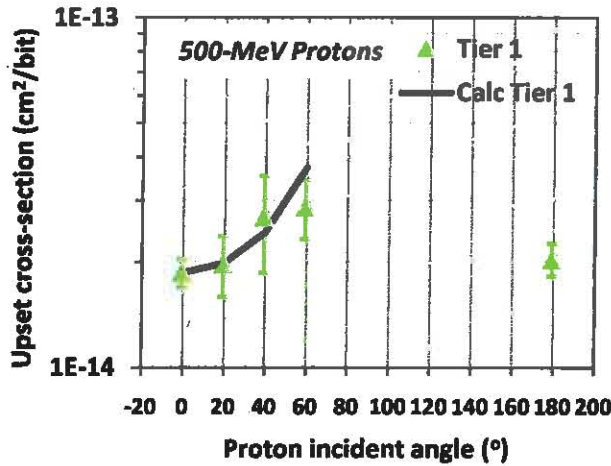


Figure 13: Experimental median upset cross-section for tier 1 of a 3DSOI SRAM as a function of the 500-MeV proton incident angle (symbols). The error bars are for ± 1 standard deviation. The solid line is the upset cross-section calculated assuming that the cross-section at an angle θ , $\sigma(\theta) = \sigma(0) / \cos \theta$.

The same analysis was repeated for the 63-MeV protons and the 14-MeV neutrons. Figure 14 and Figure 16 shows the experimental and the calculated upset cross-section for tier 1, 2 and 3 of 3D SOI SRAM as a function of the 63-MeV proton and the 14-MeV neutron incident angle. Once again, the experimental data follow the trend predicted by inverse-cosine calculation.

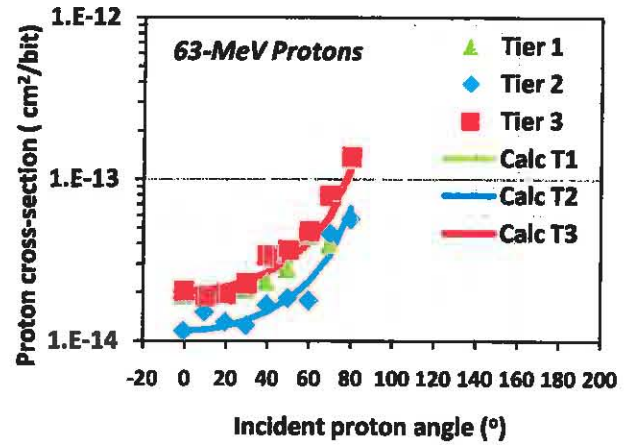


Figure 14: Experimental median upset cross-section as a function of the 63-MeV proton incident angle (symbols). The solid line is the upset cross-section calculated assuming that the cross-section at an angle θ , $\sigma(\theta) = \sigma(0) / \cos \theta$.

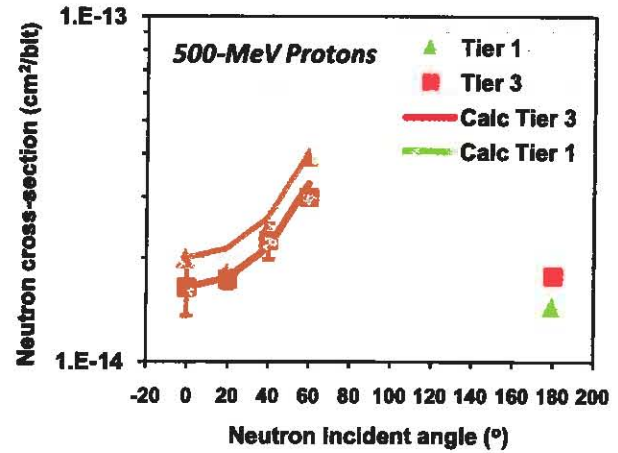


Figure 15: Experimental median upset cross-section as a function of the 14-MeV neutron incident angle (symbols). The solid line is the upset cross-section calculated assuming that the cross-section at an angle θ , $\sigma(\theta) = \sigma(0) / \cos \theta$.

C. Comparing Tiers 1, 2 and 3 of a 3DSOI SRAM

Figure 7 showed that the median upset cross-section is lower on tier 2 compared to that on tiers 1 and 3 regardless of the proton incoming angle for the series of circuits that were tested. Since the FETs on tiers 2 and 3 are inverted compared to that on tier 1, we conclude that the lower cross-section on tier 2 is not caused by the 3D integration process. Removal of the silicon substrate on tier 2 and 3 does not significantly impact the upset cross-section either. We found that the difference in upset cross-section between tiers is consistent with the variation in the FET critical dimension (W , L , t_{SOI}) observed from wafer-to-wafer and lot-to-lot in the FDSOI process as previously discussed in section V.C. As stated in section II, the 3D integration process did not

change the original FETs' electrical characteristics measured on the 2D circuit wafer before 3D integration. However, FET characteristics were different among the 2D wafers used for 3D integration because these 2D wafers were fabricated in different fabrication lots. The cross-section values measured for the three different tiers of 3D SOI SRAMs are well within the range of cross-section values measured for 2D SRAM indicating that the upset events occurring on one tier are uncorrelated with the events occurring on another tier.

In general, for all proton and neutron incident angle and for all three tiers, the data follow a normal distribution, and the standard deviation is equal to the root square of the mean of the data. Consequently, the upsets are independent from each other, and there is no significant tier-to-tier effect. These results indicate that, in the 3D SOI SRAM, proton-silicon reactions are the dominant mechanisms responsible for the upset events measured on each tier. Limited data are available in the literature for FDSOI SRAM tested with protons and neutrons at various incident angles. Our results are consistent with those published in [15] for a single-tier 0.2 μm FDSOI technology, and 14-MeV neutron angles of 0, 60 and 180°. Variations in the protons and neutron upset sensitivity between tiers is driven by variations in the sensitive volume defined by the cell FET gate width, length and the SOI thickness. Our results also show that the charge deposited by the secondary particles that are responsible for the upsets are emitted in the same direction as the primary incident particle. There is no significant change in the upset cross-section between front to back irradiation.

To further identify tier-to-tier effects, we analyzed the bitmaps showing the physical location of single event upsets induced by 500-MeV protons on tiers 1, 2 and 3. Figure 16 shows the bitmaps for each tier as well as the superimposition of the three-tier bitmaps (bitmaps were slightly offset in the + y direction to enhance the visibility of coincident upsets). Bitmaps show that the upsets are randomly distributed on each tier, and that there is no observable tier-to-tier correlation.

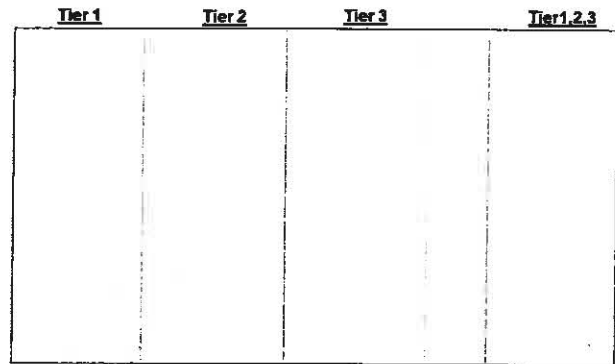


Figure 16: Bitmaps showing the physical location of single event upsets induced by 500-MeV protons at normal incidence on tier 1 in blue, tier 2 in pink and tier 3 in yellow. The upsets are randomly distributed.

We do not observe a sharp increase in the upset cross section at low proton energies on any of the tier that would be indicative of direct proton ionization effects [16],[17]. We ran SRIM [18] simulations, and found that the incident proton energy would need to be smaller than 2 MeV for the Bragg peak to fall within the active SOI regions of the three-tier SOI SRAM to observe direct proton ionization effects [19]. As shown in Table 1, the proton energy FWHM is increasing with a decrease in proton energies. Finer steps in proton energy would be required to see these effects. Loveless [13] has also shown that the variance in energy deposition can also play a meaningful role in the measured upset cross-section variation near threshold. Once again, this is because of the small sensitive volume in advanced SOI technologies.

D. Simulating the Energy Deposition by 500-MeV protons

Simulations were performed using the Monte Carlo Radiative Energy Deposition (MRED) code [20]. MRED is a simulation tool that calculates the energy deposited by radiation in microelectronic devices based on the Geant4 libraries [21]. Clemens et al [22] have shown that the presence of high Z materials increases the proton-induced charge collection cross-sections for high charge collection events. The mechanism for this effect was shown to be a proton-induced fission event as validated with Monte Carlo simulations. Simulations were run to compare the energy deposited by 500-MeV protons in the sensitive volume of the SRAM FET on tier 1, 2 and 3 for normal incident angles (front side irradiation) and 180° (back side irradiation). Figure 17 gives a description of the layers (material and depth) that matched the 3DIC process, and that were used for the simulations. The thickness of tungsten layer was calculated by looking at the fractional area of the contact and via by the depth with respect to the sensitive area.

	Layer Name	MRED Material	Depth (nm)
Tier 3	Al-Cu (Cu < 0.8%)	Aluminum	2000
	SiO ₂	SiO ₂	600
	Sensitive Detector	Silicon	40
	M1-Active Contact	Tungsten	50.63
	Co-silided Poly	Silicon	150
	M1-Poly Contact	Tungsten	13.71
	SiO ₂	SiO ₂	800
	Metal 1 (M1)	Aluminum	630
	M1-M2 Via	Tungsten	31.65
	SiO ₂	SiO ₂	1000
	Metal 2 (M2)	Aluminum	630
	SiO ₂	SiO ₂	1000
	Metal 3 (M3)	Aluminum	630
	SiO ₂	SiO ₂	2100
	Back Gate Metal	Aluminum	630
Tier 2	SiO ₂	SiO ₂	600
	Sensitive Detector	Silicon	40
	M1-Active Contact	Tungsten	50.63
	Co-silided Poly	Silicon	150
	M1-Poly Contact	Tungsten	13.71
	SiO ₂	SiO ₂	800
	Metal 1 (M1)	Aluminum	630
	M1-M2 Via	Tungsten	31.65
	SiO ₂	SiO ₂	1000
	Metal 2 (M2)	Aluminum	630
	SiO ₂	SiO ₂	1000
	Metal 3 (M3)	Aluminum	630
	SiO ₂	SiO ₂	2100
	Metal 2 (M2)	Aluminum	630
	SiO ₂	SiO ₂	1000
Tier 1	M1-M2 Via	Tungsten	31.65
	Metal 1 (M1)	Aluminum	630
	SiO ₂	SiO ₂	800
	M1-Poly Contact	Tungsten	13.71
	Co-silided Poly	Silicon	150
	M1-Active Contact	Tungsten	31.65
	Sensitive Detector	Silicon	40
	SiO ₂	SiO ₂	400
	Substrate	Silicon	10 μ m

Figure 17: Description of the layers used to simulate the energy deposited by 500-MeV protons with MRED. The layers match the materials and thickness of the inverter of the SET collecting circuit.

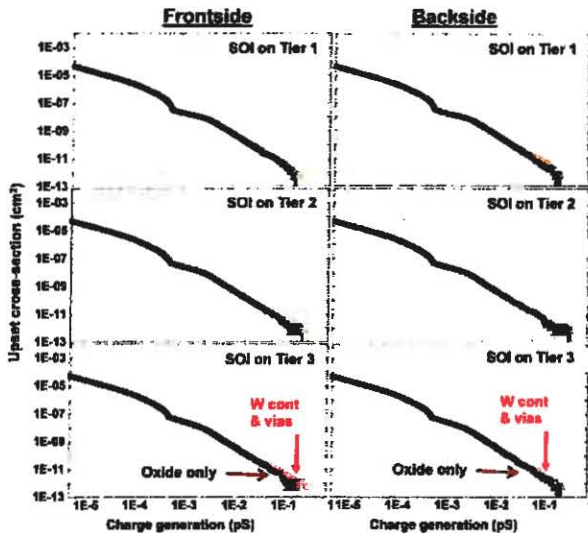


Figure 18: Results from MRED simulations showing the cross-sections as a function of the charge generated by 500-MeV protons in the sensitive SOI device layer for a cell FET in tier 1, 2 and 3 of the 3D SOI SRAM. Results are also shown for a control case where the tungsten (W) contact and vias were replaced by SiO₂ (oxide).

Simulation results show that the tungsten layers had no significant effect on tier-to-tier energy deposition. Also, the back side and front side simulations show no significant difference in tier-to-tier energy deposition. These simulation results are consistent with the experimental data.

VI. CONCLUSION

Radiation effects are presented for the first time for vertically integrated 3 x 64-kb SOI SRAM circuits. 3D SOI SRAM were fabricated using Lincoln-3D technology integrating vertically three fully-fabricated 2D circuit wafers that are interconnected with 1.75- μ m through-oxide vias. The total 3D circuit is 20- μ m thick.

The 3D SOI SRAMs are tolerant to ionizing radiation induced by 500-MeV protons. Testing with protons with energies between 4.8 and 500MeV and 14-MeV neutrons yielded similar results. The upset cross-section for 3D SOI SRAM is similar for all tiers, and it is also similar to that for single-tier 2D SRAM. The other tiers can be effectively modeled as a modified backend-of-line stack. Differences between tiers were directly attributed to variations in the critical dimensions of the sensitive volume defined by the device width, gate length and SOI thickness.

Angular effects measured with protons and neutrons were also directly attributed to the change in the particle path length within the sensitive volume. The upset cross-section has an inverse-cosine dependence on the neutron/protons incident angle. No tier-to-tier effects were identified. Monte Carlo simulations confirmed the experimental results.

3D integration is an effective novel approach to fabricating high-density, high-performance, integrated circuits. This work demonstrates that radiation-hardened vertically integrated 3D circuits can be suitable for space and military applications.

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